

RoHS Compliant Product
A suffix of "-C" specifies halogen free

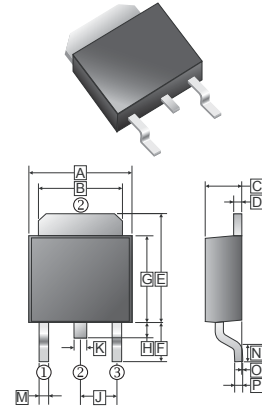
DESCRIPTION

These miniature surface mount MOSFETs utilize high cell density process. Low $R_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Miniature TO-252 surface mount package saves board space.
- High power and current handling capability.
- Extended V_{GS} range (± 25) for battery pack applications.

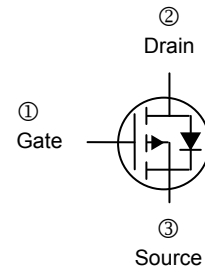
TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30	REF.
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			

PACKAGE INFORMATION

Package	MPQ	LeaderSize
TO-252	2.5K	13' inch



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ¹	$I_D @ T_A=25^\circ\text{C}$	61	A
Pulsed Drain Current ²	I_{DM}	± 40	A
Continuous Source Current (Diode Conduction) ¹	I_S	-30	A
Total Power Dissipation ¹	$P_D @ T_A=25^\circ\text{C}$	50	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	$^\circ\text{C}$
THERMAL RESISTANCE RATINGS			
Maximum Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	50	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3.0	$^\circ\text{C} / \text{W}$

Notes :

- 1 Surface Mounted on 1" x 1" FR4 Board.
- 2 Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-		$V_{DS} = V_{GS}, I_D = -250 \mu A$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0V, V_{GS} = \pm 25V$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -24V, V_{GS} = 0V$
		-	-	-5		$V_{DS} = -24V, V_{GS} = 0V, T_J = 55^\circ C$
On-State Drain Current ¹	$I_{D(on)}$	-41	-	-	A	$V_{DS} = -5V, V_{GS} = -10V$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	9	m Ω	$V_{GS} = -10V, I_D = -61A$
		-	-	13		$V_{GS} = -4.5V, I_D = -51A$
Forward Transconductance ¹	g_{fs}	-	31	-	S	$V_{DS} = -15V, I_D = -61A$
Diode Forward Voltage	V_{SD}	-	-0.7	-	V	$I_S = -41 A, V_{GS} = 0 V$
Dynamic ²						
Total Gate Charge	Q_g	-	37	-	nC	$V_{DS} = -15 V$ $V_{GS} = -4.5 V$ $I_D = -61 A$
Gate-Source Charge	Q_{gs}	-	10	-		
Gate-Drain Charge	Q_{gd}	-	14.5	-		
Switching						
Turn-on Delay Time	$T_{d(on)}$	-	15	-	nS	$V_{DD} = -15 V$ $I_D = -41 A$ $V_{GEN} = -10 V$ $R_L = 15 \Omega$ $R_G = 6 \Omega$
Rise Time	T_r	-	12	-		
Turn-off Delay Time	$T_{d(off)}$	-	62	-		
Fall Time	T_f	-	46	-		

Notes

- 1 Pulse test : Pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.
- 2 Guaranteed by design, not subject to production testing.